ACHARYA

ACHARYA INSTITUTE OF TECHNOLOGY

NAAC ACCREDITED NBA

Department of ECE

Skill Development Program on

MEMORY DESIGN & VERIFICATION USING VERILOG

under C2S Programme

18th - 22nd August 2025 | 9.00 AM to 4.30 PM

VLSI Lab, ECE Department, Acharya Campus

IN ASSOCIATION WITH

IEEE BANGALORE SECTION

About the Program

This program is designed to equip participants with practical, hands-on skills in memory design, leveraging industry-standard tools. It focuses on bridging the gap between theory and application by offering real-world experience in designing and simulating digital circuits. The program also aims to foster a deep understanding of how digital components interact and integrate seamlessly within modern VLSI (Very Large Scale Integration) systems.

Objectives of the Program

- To provide practical, hands-on skills in memory design using industry-standard tools.
- To facilitate an understanding of the interplay and seamless integration between digital components in modern VLSI systems.

Expected Outcomes of the Program

- Simulation and synthesis of Memory circuits using Verilog.
- Performance analysis of Memory Designs in-terms of Area, Power and Speed.
- Team Building and Communication skills through project-based learning and presentation.

Target Audience: ECE Students

Committee Members

ADVISORY COMMITTEE

- Dr. Marigowda C K, Principal of AIT, Bengaluru
- Dr Rajeswari, Dean Academics, HOD.ECE, AIT, Bengaluru
- Dr.Anil Kumar Ramesh, Head, R & D, Dover India Private Ltd., Bengaluru
- Dr. S K Murthy, Patent Counsel, Intel Technologies, Bengaluru
- Dr. H V Ravish Aradhya, Professor, RV college of Engineering, Bengaluru
- Mr. M Venkatash, CEO, Technocarve Solutions, Bengaluru
- Mr. Manjunath Srinivasaiah, Project Manager, Robert Bosch, Bengaluru

CONVENER

- Dr. Rajeswari, Dean Academics, HOD.ECE, AIT, Bengaluru

TECHNICAL TEAM

- Mr. Vinod K R, Lab Instructor, Dept of ECE, AIT
- Mrs. Manjula S, Lab Instructor, Dept of ECE, AIT

EVENT COORDINATORS

- Mrs. Sumangala S J
- Dr. Nikita Kar Choudhary

Resource Persons Details

Mr. Jaganath Rajendra
Designation: Principal,
Analogue and Mixed Signal IC Design Engineer at Salience Labs, Oxford

Dr. Jayalaxmi H
Designation: Associate Professor,
Dept of ECE, AIT

Dr. Asha C.N
Designation: Associate Professor,
Dept of ECE, AIT

Dr.Nagapushpa K.P
Designation: Assistant Professor,
Dept of ECE, AIT

Prof. Veena Sanath Kumar
Designation: Assistant Professor,
Dept of ECE, AIT

Dr. Munnavar Sheriff I
Designation: Assistant Professor,
Dept. of ECE, AIT

Prof. Mrs.Sumangala S J
Designation: Assistant Professor,
Dept. of ECE, AIT

Dr. Nikita Kar Chowdhury
Designation: Assistant Professor,
Dept. of ECE, AIT

Note:
1. No Registration Fee
2. E-Certificate will be provided upon successful completion of the assessment during the program.

Acharya Institute of Technology

Acharya Dr. S. Radhakrishnan Road, Acharya P.O
Soladevanahalli, Bangalore - 560107, Karnataka, India.

LOCATE US

Event Coordinator

Mrs. Sumangala S J